

REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 54-57 are pending in this application. Claims 48-53 are canceled by the present response without prejudice. Claims 1-47 were previously canceled without prejudice. Claims 54-47 were rejected under 35 U.S.C. § 112, second paragraph. Claims 48-50, 52, 54, and 56 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. patent 6,326,268 to Park et al. (hereinafter “Park”) in view of U.S. patent 6,448,606 to Yu et al. (herein “Yu ‘606’”). Claims 51, 53, and 57 were rejected under 35 U.S.C. § 103(a) as unpatentable over Park and Yu ‘606 and further in view of U.S. patent 6,265,293 to Yu (herein “Yu ‘293’”). Claim 55 was rejected under 35 U.S.C. 103(a) as unpatentable over Park and Yu ‘606 as applied to claim 54, and further in view of U.S. patent 6,265,293 to Hurley et al. (herein “Hurley”).

Initially, applicants note that the outstanding rejections now rely on newly cited U.S. patent 6,448,606 to Yu ‘606. However, applicants note that at this time that reference has not been formally made of record. That is, Yu ‘606 has not been indicated on a form PTO-892. Applicants respectfully request that reference clearly be made of record by being listed on a form PTO-892.

Addressing now the rejection of claims 54-57 under 35 U.S.C. § 112, second paragraph, that rejection is traversed by the present response. Applicants respectfully submit the claim language in claim 54 is definite, and the basis for the outstanding rejection is not at all understood. The rejection of claims 54-57 states:

Claim 54 recites the phrases “a memory cell having a first channel and a first gate insulating film ... the memory cell being sandwiched between the first shallow trench isolation regions ...” and “a transistor having a second channel and a second gate insulating ... the transistor being sandwiched between the second shallow trench isolation regions.” This recitation carries an unclear meaning because it implies as if a

memory cell and a transistor are distinctive structures, but actually meaning the same.¹

First, applicants note that in the claims the memory cell and the transistor are in fact distinct structures. As a non-limiting example, the “memory cell” corresponds to an element formed by the process of Figures 12A to 27A and the “transistor” corresponds to an element formed by the process of Figs. 12B to 27B or an element formed by the process of Figs. 12C to 27C.

Applicants respectfully submit that claim 54 is clear that the memory cell and the transistor are distinct structures. It is unclear on what basis the outstanding rejection interprets the claims as “actually meaning the same”. The claim language is believed to clearly recite a memory cell and transistor as distinct structures. Thus, each of claims 54-57 is believed to be in full compliance with all requirements under 35 U.S.C. § 112, second paragraph.

Addressing now each of the above-noted prior art rejections, applicants respectfully submit claims 54-57 distinguish over the applied art, claims 48-53 being canceled by the present response without prejudice.

With respect to the rejection of claim 54 as unpatentable over Park in view of Yu ‘606, claim 54 is believed to distinguish over that applied art.

Applicants respectfully submit no combination of teachings of Park in view of Yu ‘606 discloses the claimed features of the “first concave portions of the first shallow trench isolation regions”, and specifically “wherein the first concave portions are formed *above the charge storage layer*” (emphasis added). That feature positively recited in claim 54 is believed to clearly distinguish over the applied art.

With respect to the above-noted feature, the outstanding Office Action states:

¹ Office Action of August 24, 2004, page 2.

Fig. 7 of Park shows the most aspect of the instant invention except “the shallow trench isolation regions include concave portions on upper ends” and “the concave portions are formed above the charge storage layer.” Fig. 5b of Yu shows “the shallow trench isolation regions (318B) include concave portions on upper ends” and “the concave portions are formed above the charged storage layer (306B).”²

The above-noted basis for the outstanding rejection is traversed as the relied upon teachings in Yu ‘606 do not meet the claimed features.

As shown as a non-limiting example in Figure 1 of the present specification, according to the above-noted claim feature, concave portions formed on the upper ends of the shallow trench isolation region 13 of the memory cell are located *above* the charge storing layer 11.

In contrast to such a claimed feature, as shown in Figure 5B of Yu ‘606, concave portions 320B are in contact with a charge storage layer 306B, and thereby are not formed above the charge storage layer 306B. The basis for the outstanding rejection misinterprets the teachings in Yu ‘606 relative to the claimed features. Yu ‘606 simply does not teach or suggest concave portions formed above a charge storage layer, as recited in claims 54-57. In Yu ‘606 the concave portions 320B are in contact with the charge storage layer and thus are not above the charge storage layer 306B.

Thereby, independent claim 54, and the claims dependent therefrom, patentably distinguish over Park in view of Yu ‘606.

Moreover, no teachings in Yu ‘293 or Hurley overcome the above-noted deficiencies of Park in view of Yu ‘606.

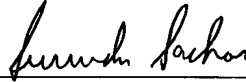
In view of these foregoing comments, applicants respectfully submit claims 54-57 distinguish over the applied art.

² Office Action of August 24, 2004, page 3, penultimate paragraph.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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